CLAIMS:

1.   A logic emulation system for emulating a logic under verification, comprising:

a synthesis unit for synthesizing a multi-value supporting logic for said logic under verification;

a logic compile unit for assigning said multi-value supporting logic to a programmable gate array; and

an emulation unit for performing multi-value supporting logic emulation using the programmable gate array to which said compile unit assigns said multi-value supporting logic.

2.   A logic emulation system according to claim 1, wherein:

said synthesis unit implements one logic signal line for transmitting a multi-valued logic signal by a plurality of physical signal lines to synthesize the logic.

3.   A logic emulation system according to claim 1, wherein:

said synthesis unit includes a value information storage unit for storing value information, and performs multi-valued synthesis corresponding to a value stored in said value information storage unit.

4.   A logic emulation system according to claim 1, wherein:

said synthesis unit performs logic synthesis

using information on a logic cell stored in a cell library for multi-value supporting synthesis.

5.   A logic emulation system according to claim 1, wherein:

said synthesis unit reads a specifying value that specifies with which value the synthesis is performed, calculates the number of logic signal lines in a logic circuit as Log_2 a raised integer of (the specifying value), and logically connects the respective signal lines.

6.   A logic emulation system according to claim 1, wherein:

said system performs one logic gate operation using a programmable device in said programmable gate array in a one-input/one-output configuration, a one-input/multiple-output configuration, a multiple-input/one-output configuration, or a multiple input/multiple output configuration to implement a multi-valued logic operation.

7.   A multi-valued logic emulation system for emulating a logic under verification, said system having an information processing unit and a logic emulator including a plurality of rewritable logic devices constituting a logic circuit, wherein said information processing unit comprises:

a first storage unit for storing information on a logic circuit under emulation;

a second storage unit for storing value

information on a logic value of said logic circuit; and

a processing unit for calculating a required number of physical signal lines from said logic circuit information and said value information, and mapping and compiling said logic circuit in accordance with said number of physical signal lines to create a multi-valued emulation program.

8.   A multi-valued logic emulation system according to claim 7, wherein:

said information processing unit calculates a required number of physical signal lines using said value information by the following equation:

Number n of Physical Signal Lines = Log_2 Raised Integer of Value Information.

9.   A multi-valued logic emulation system according to claim 7, wherein said information processing unit further comprises:

an input device for inputting said value information.

10.   A multi-value supporting logic emulation method executed by an information processing unit and a logic emulator including a plurality of writable logic devices, said method comprising the steps of:

said information processing unit reading information on a logic circuit to be emulated;

said information processing unit storing value information on a logic value of said logic circuit in a storage unit;

said information processing unit calculating a required number of physical signal lines from said read logic circuit information and said value information; and

said information processing unit creating a multi-valued logic emulation program for said logic circuit in accordance with the number of physical signal lines.

11.   A multi-value supporting logic emulation method according to claim 10, wherein:

said information processing unit calculates a required number of physical lines using said value information by the following equation:

Number $\underline{n}$ of Physical Signal Lines = Log_2 Raised Integer of Value Information.

12.   A multi-value supporting logic emulation method according to claim 11, wherein:

said information processing unit acquires said value information using an input device.